

Design of a Two-layer SIW Power Divider with Slot Aperture Y-Junction for Enhanced Narrowband Isolation

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ABSTRACT

This study presents a 3 dB power divider based on a two-layer Substrate Integrated Waveguide (SIW) structure designed to achieve high isolation and optimal return loss at both output ports while maintaining low insertion loss. The initial configuration uses a conventional Y-junction SIW power divider, which demonstrates limited isolation between output ports. A rectangular slot was incorporated at the Y-junction, significantly enhancing isolation. Although this adjustment introduced some insertion loss, a second substrate layer with a copper patch was added above the slot, effectively minimizing insertion loss and preserving strong isolation without the need for an isolation resistor. The resistor-free design simplifies fabrication and improves reliability by avoiding components that may fail under high power conditions. Due to fabrication constraints, the power divider is optimized for performance at two center frequencies, 12 GHz and 24 GHz, with prototyping focused on 12 GHz. Simulated and measured results at 12 GHz are in close agreement, confirming measured isolation performance with at least 10 dB of isolation over a fractional bandwidth of 9.9%. While this narrowband design may not suit all applications, it offers high precision for systems

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that require strict frequency isolation, making it especially advantageous for targeted narrowband applications where isolation and reliability are critical.

Keywords: 3 dB power divider, bi-layered substrate, slot aperture, substrate integrated waveguide

INTRODUCTION

In microwave systems, power dividers play a crucial role by enabling the division of signals into predetermined sub-paths. Depending on the specific application, these divisions can occur with equal or varying power levels. Historically, traditional waveguide structures were commonly employed to perform this function due to their ability to handle high-frequency signals efficiently. However, these conventional waveguides had significant drawbacks. They were often large and required complex and costly manufacturing processes, which made them impractical for widespread use, particularly in mass production environments where compactness and cost-effectiveness are key considerations. Power dividers have been widely implemented in various subsystems such as antenna feeding networks, interferometers, and other critical components that are integral to microwave systems.

In more recent years, microstrip-based power dividers have become increasingly preferred in many applications. This shift is primarily due to the planar structure of microstrip technology, which offers excellent compatibility with modern printed circuit board (PCB) designs. Microstrip-based designs also allow for easier integration into electronic devices, which often need to be both compact and lightweight to meet industry standards for portability and efficiency. The T-junction power divider, for example, is one of the most popular types of microstrip-based power dividers. Its appeal lies in its simple design and relatively straightforward manufacturing process. Despite these advantages, the T-junction power divider has some inherent limitations. Specifically, it is typically narrowband in nature, as it is challenging to match the impedance at the output ports, which often results in poor return loss and limited isolation performance (Chen et al., 2010; He et al., 2013).

An alternative structure known as the Wilkinson power divider has been developed to address the shortcomings of the T-junction design. This design offers several advantages, including improved isolation between the output ports and a broader operational bandwidth. Furthermore, the Wilkinson power divider is relatively compact, making it well-suited for applications requiring space-efficient components (Kao et al., 2012; Feng et al., 2017). It achieves these benefits by utilizing isolation resistors, crucial in enhancing isolation performance. Additionally, its compact form factor allows it to be integrated into modern microwave systems where space is at a premium (Peng et al., 2013).

A relatively new method for implementing Wilkinson power dividers is using Substrate Integrated Waveguides (SIW). SIW technology combines the high-power handling

capabilities of traditional waveguides with the low-loss characteristics of microstrip circuits, making it an ideal solution for modern high-frequency applications. One of the significant advantages of SIW is its ability to maintain the performance characteristics of conventional waveguides while offering the compactness and ease of integration associated with planar structures (Duraismy et al., 2022). Over the last decade, SIW technology has been widely adopted in designing various microwave components, such as tunable filters, amplifiers, couplers, and filters (Shen et al., 2021).

Further advancements in this field have focused on improving isolation performance in SIW-based Wilkinson power dividers. A notable development is the Half-Mode SIW (HMSIW) Wilkinson power divider. The HMSIW design reduces the overall size of the power divider while maintaining its performance characteristics. However, this design still relies on the use of isolation resistors, which, although improving isolation, can introduce unwanted cross-coupling effects and radiation losses due to the discontinuities in the structure (Smith & Abhari, 2009; Kim et al., 2010). These limitations have led to further exploration of alternative approaches, one of which involves the construction of ring-based power dividers within the SIW structure. This design aims to mitigate the disadvantages associated with the HMSIW structure by compensating for the losses introduced by isolation resistors (Djerafi et al., 2013; Djerafi et al., 2014; Moulay & Djerafi, 2018).

Narrowband power dividers are particularly useful in applications that benefit from precise signal isolation over specific frequency bands. For instance, phased array and beam-steering systems often rely on narrowband power dividers to achieve focused frequency isolation, ensuring stability and minimal interference within targeted operating ranges. These designs provide effective isolation within a specified band, making them well-suited for applications that do not require broad frequency isolation but benefit from precise control within a limited range (Zarghami & Hayati, 2022).

This study introduces a novel SIW power divider that improves isolation but eliminates the need for isolation resistors using a two-layer structure. The design starts with a conventional Y-junction SIW power divider and incorporates a rectangular slot aperture at the junction on the lower layer to direct signal propagation forward, enhancing isolation performance. To address the increased insertion loss caused by the slot, a second substrate layer with a precisely aligned copper patch is added, enabling improved isolation while controlling insertion loss. This resistor-free configuration simplifies the fabrication process and enhances durability, making it well-suited for applications that require reliable isolation without added component complexity.

The proposed power divider is demonstrated at two frequency bands centered at 12 GHz and 24 GHz, targeting applications that require focused isolation within specific narrow frequency ranges. This work suggests that the proposed resistor-free, dual-layer SIW power divider provides a practical, high-performance solution for compact microwave systems where isolation, compactness, and ease of integration are critical.

METHODOLOGY

This study explores the design of an SIW power divider operating at two center frequencies, 12 GHz and 24 GHz. The design process begins with a conventional Y-junction SIW power divider, as illustrated in Figure 1.

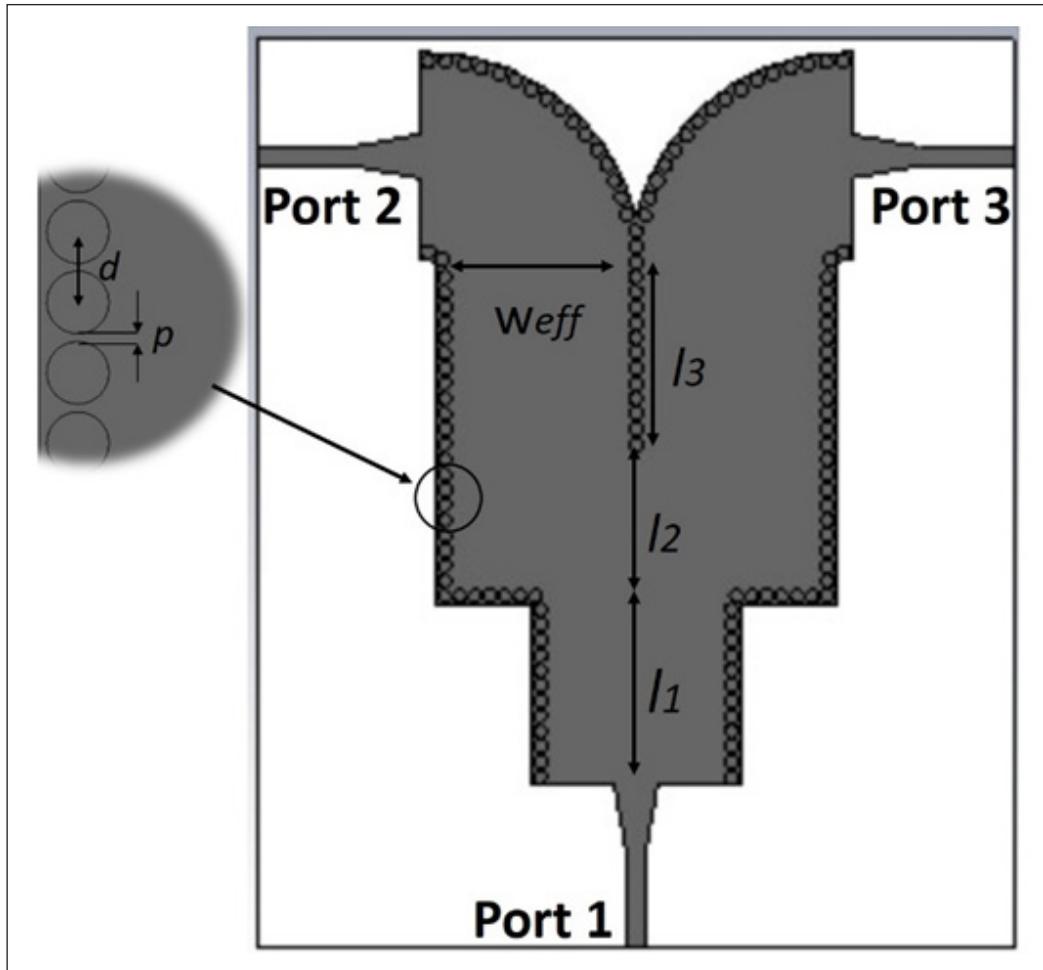


Figure 1. Topology of the conventional Y-junction SIW power divider

This conventional design was previously introduced in a 24 GHz SIW power splitter developed for six-port short-range radar-based sensors (Tan et al., 2016). In that study, the design used a basic Y-junction layout focused on simulations, with output ports positioned side by side. Practical considerations for physical measurements, such as SMA connector placement, were not included, as the design was intended only for simulation purposes.

The current study introduces a bending SIW structure at both output ports to address these limitations. This modification repositions the output ports on opposite sides of the

divider, allowing for easier connection to SMA connectors for practical measurements. This configuration enhances accessibility and supports physical prototyping and testing without altering the fundamental Y-junction layout.

Several critical parameters influence the design and performance of the SIW structure, including the effective width (W_{eff}), the diameter of the via holes (d), and the separation between via holes (p). Additionally, the lengths of sections within the Y-junction, designated as l_1 , l_2 and l_3 , are essential in tuning the design to the desired frequencies. Among these, the length l_2 is particularly significant, as it directly influences the operating frequency, targeted at 12 GHz and 24 GHz.

The dimensions of the via holes and their spacing are designed to meet specific criteria to ensure efficient wave propagation and prevent unwanted modes. According to Xu and Wu (2005), the ratio of via-hole separation to cutoff wavelength (p/λ_c) should be less than 0.25. Additionally, the diameter (d) must be smaller than the spacing (p), with the following condition satisfied (Equation 1).

$$d < p < 2d \quad [1]$$

These constraints ensure that the structure supports the desired TE_{m0} modes, particularly the dominant TE_{10} mode, which is essential for stability at both targeted frequencies (Cassivi et al., 2002).

Empirical formulas based on established research are used to estimate initial values for these critical parameters (Cassivi et al., 2002; Deslandes & Wu, 2006). The cutoff frequency for the TE_{10} mode is determined by using Equation 2:

$$f_{c(TE10)} = \frac{c}{2\sqrt{\epsilon_r}} \cdot \left(W - \frac{d^2}{0.95 \times p} \right)^{-1} \quad [2]$$

Where c is the speed of light, ϵ_r is the relative permittivity of the substrate, W is the width of the SIW, d is the diameter of the via holes, and p is the separation between via holes. This formula is crucial in aligning the cutoff frequencies with the target operating frequencies of 12 GHz and 24 GHz.

The effective width of the SIW (W_{eff}) is calculated using Equation 3:

$$W_{eff} = W - \frac{d^2}{0.95 \times p} \quad [3]$$

This effective width influences the waveguide's propagation characteristics, affecting the distribution of electromagnetic fields within the SIW structure.

Figure 2 shows the proposed power divider design, which introduces a rectangular slot aperture at the Y-junction of the conventional SIW structure to enhance isolation by

disrupting the electric field distribution. This slot, along with a rectangular metallic patch positioned directly above it, effectively reduces coupling between output ports, thereby improving isolation. The key parameters of this slot include its position (S_p), width (S_w) and length (S_l), which are optimized to achieve maximum isolation performance.

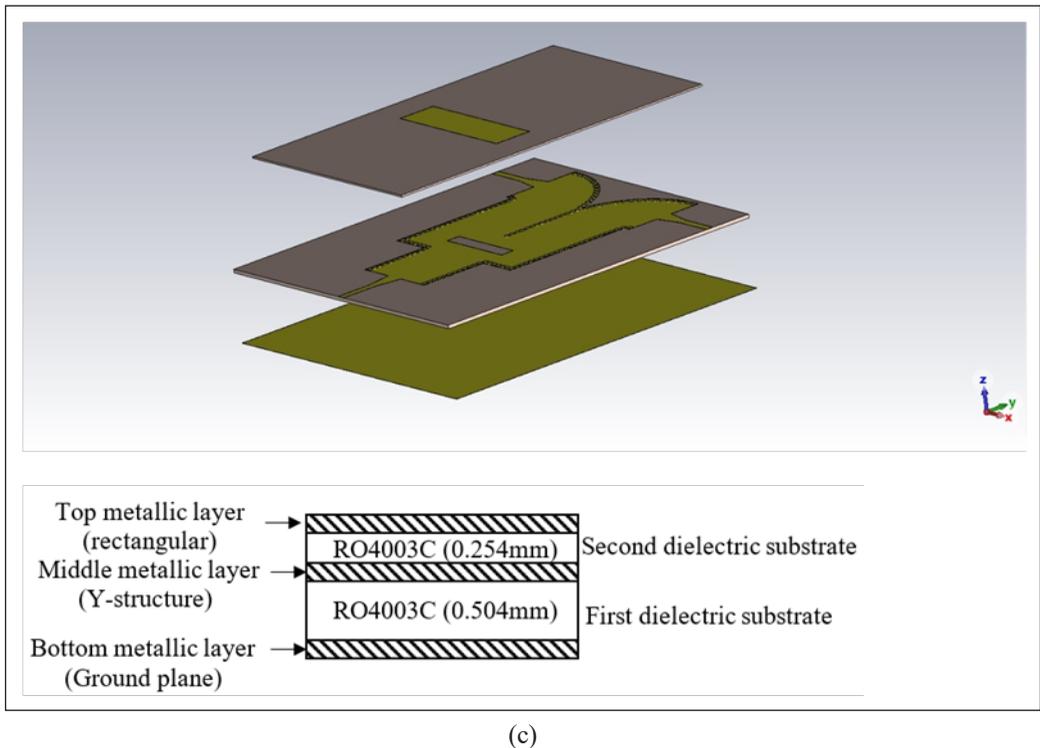
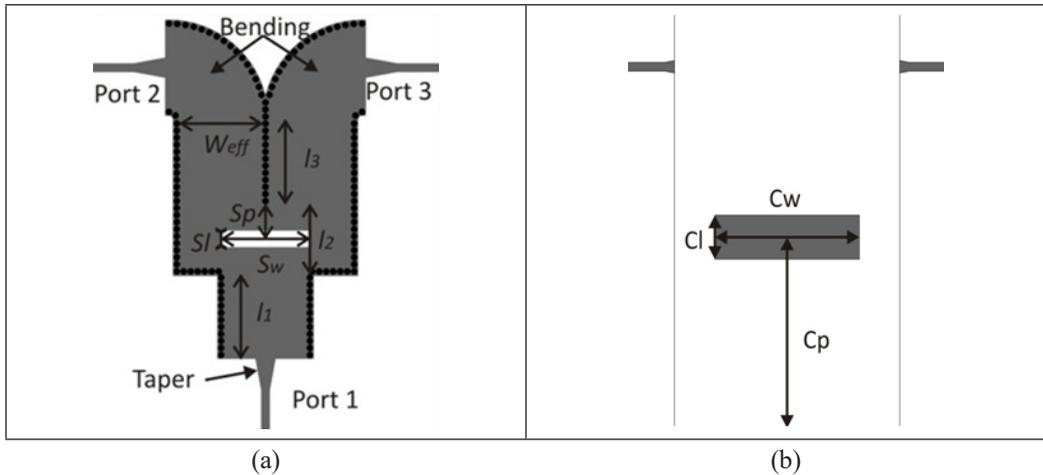


Figure 2. Configuration of the proposed SIW power divider (a) front view of the proposed Y-structure with slot aperture (b) front view (with two layers) (c) exploded view

However, the addition of the slot can result in increased insertion loss. A thin dielectric substrate layer with a rectangular metallic patch is placed directly above the slot to counter this. This patch, precisely aligned over the slot, reflects the signal into the structure, thereby minimizing insertion loss while preserving the improved isolation. The parameters of this top rectangular metallic patch, such as its position (C_p), width (C_w), and length (C_l), are carefully optimized to align with the slot, ensuring effective signal reflection and low insertion loss.

The modified structure combines the optimized slot aperture and the patch-covered layer to achieve a balance of high isolation and low insertion loss. It is suitable for high-frequency applications that demand effective power division and robust isolation. The careful alignment of slot and patch parameters enables the structure to address isolation and insertion loss, providing a practical and efficient solution for high-performance microwave systems.

The proposed power divider is designed using the RO4003C substrate, chosen for its low-loss dielectric properties, which are ideal for high-frequency applications. The bottom layer has a standard thickness of 0.508 mm to provide robust support for the waveguide. The top layer, designed with the same RO4003C substrate but a thinner profile of 0.254 mm, is used to improve insertion loss, reduce overall bulk, and enhance the electromagnetic performance of the power divider by minimizing signal loss.

The designs are validated at two frequency ranges, 12 GHz and 24 GHz, using CST Microwave Studio, a commercially available electromagnetic simulation software, to demonstrate the effectiveness of the proposed structure. After optimizing the designs at these center frequencies, the final dimensions of each design are provided in Table 1.

Table 1
Dimensions of conventional and proposed SIW power divider

Parameter	Description	Conventional (single layer)	Proposed (two-layer)	Conventional (single layer)	Proposed (two-layer)
f	Centre Frequency (GHz)	12	12	24	24
W_{eff}	Effective width of the Substrate Integrated Waveguide (mm)	10.6	10.6	4.5	4.5
l_1	Length of various sections of the Y-junction(mm)	10.6	10.6	4.4	4.4
l_2	Length of various sections of the Y-junction(mm)	9.3	9.3	3.4	3.4
l_3	Length of various sections of the Y-junction(mm)	10.7	10.7	4.4	4.4
d	Diameter of the via holes(mm)	0.8	0.8	0.5	0.5

Table 1 (continue)

Parameter	Description	Conventional (single layer)	Proposed (two-layer)	Conventional (single layer)	Proposed (two-layer)
p	Pitch (separation) between the via holes(mm)	0.9	0.9	0.6	0.6
C_l	Length of the top metallic layer(mm)	Not available	5.9	Not available	2.7
C_w	Width of the top metallic layer(mm)	Not available	20.2	Not available	8.5
C_p	Position of the top metallic layer(mm)	Not available	21.7	Not available	10.15
S_l	Length of the rectangular slot on the middle metallic layer(mm)	Not available	2.1	Not available	0.6
S_w	Width of the rectangular slot on the middle metallic layer(mm)	Not available	11.4	Not available	5.5
S_p	Position of the rectangular slot on the middle metallic layer(mm)	Not available	3.4	Not available	1.9

RESULTS AND DISCUSSION

Initial simulations at 12 GHz and 24 GHz were conducted to examine the electric field (E-field) distribution and to assess the effect of the two-layer design versus a single-layer configuration. Figure 3 shows the E-field distribution at 12 GHz and 24 GHz, illustrating the critical role of the rectangular slot and top substrate layer in achieving improved isolation and reducing insertion loss.

In the single-layer SIW configuration, signal propagation from port 1 to port 2 is less isolated, with noticeable energy leakage to port 3 due to the Y-junction structure. However, in the two-layer SIW power divider, the rectangular slot acts as an aperture that guides signal propagation outward through the slot, while the top substrate layer minimizes signal loss. When the slot is on top of the SIW, controlled radiation occurs, as the electric current is directed along the slot, resulting in a specific current distribution around it. This current distribution is influenced by the position of the slot (denoted by S_p), which affects the amount of radiated power and, subsequently, the device's overall isolation and transmission characteristics.

The structure within the l_2 section of the power divider can be approximated as a series impedance. In this configuration, adding a top metallic layer over the slot establishes a resonant condition, ensuring that the device's impedance is primarily resistive with minimal reactive contribution. By reducing reactive impedance, this design promotes efficient signal propagation and achieves the desired isolation between output ports.

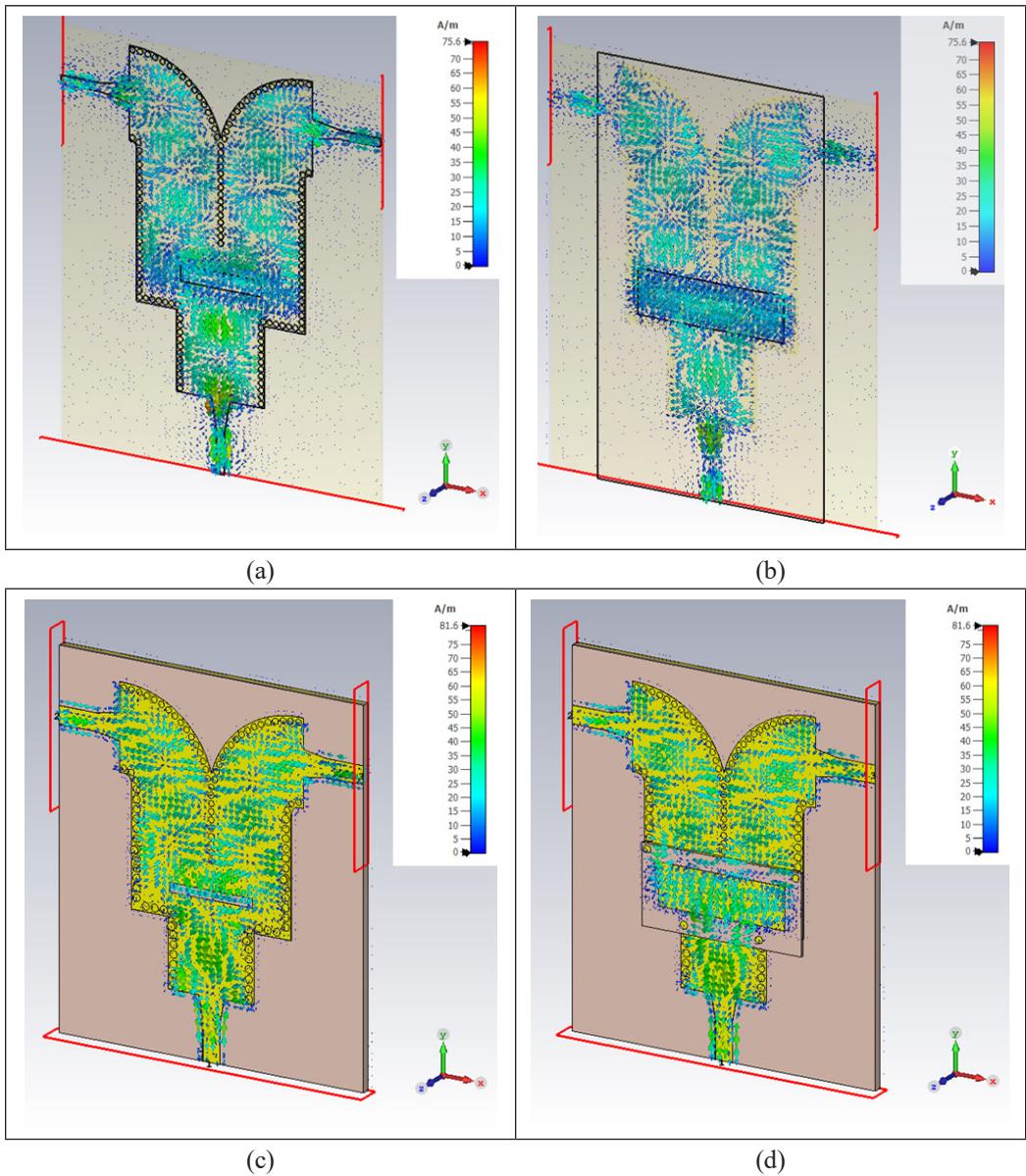
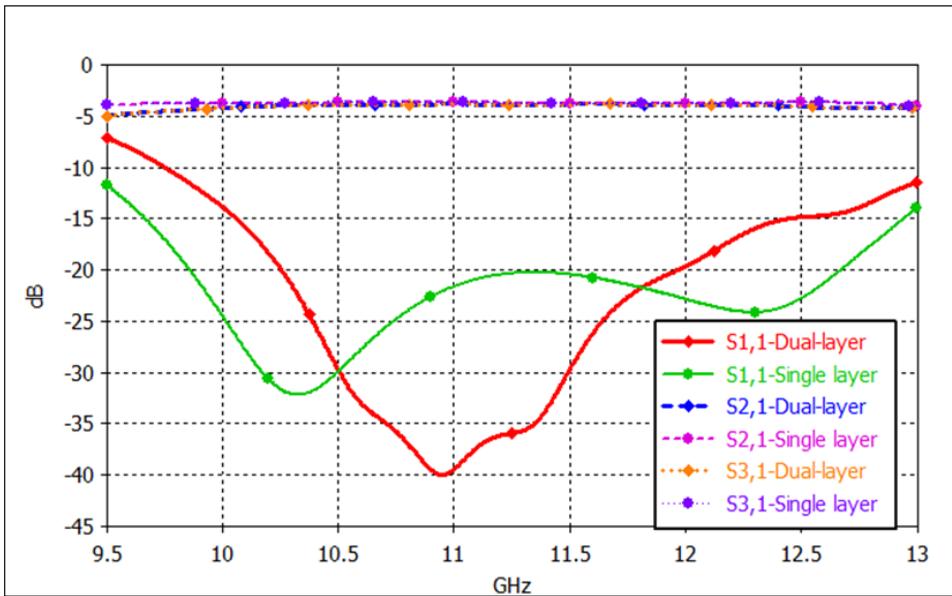


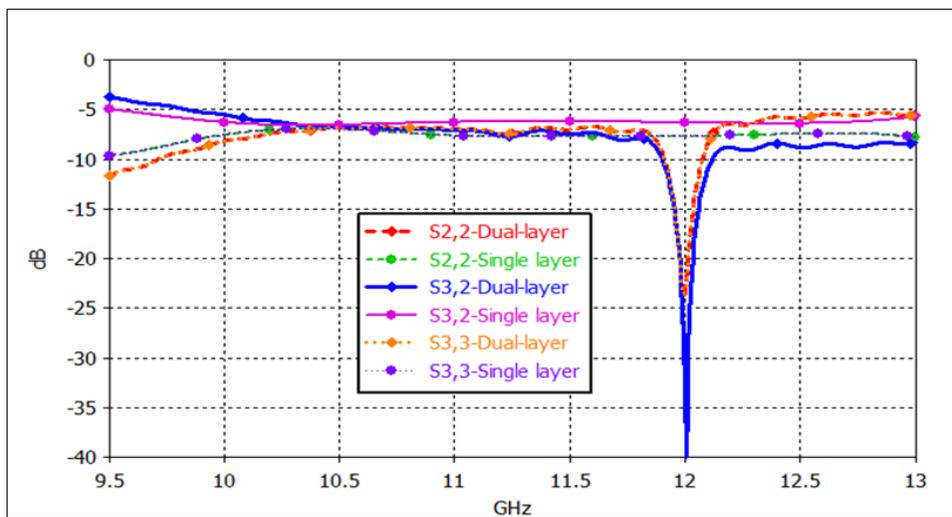
Figure 3. E-field distribution for (a) 12 GHz (single), (b) 12 GHz (dual), (c) 24 GHz (single), and (d) 24 GHz (dual)

The coordinated interaction between the slot, top substrate layer, and metallic components effectively isolates the SIW power divider. This design ensures minimal signal loss while maintaining high isolation levels, even with minor fabrication imperfections, making the SIW power divider a reliable solution for high-frequency applications.

The single-layer and dual-layer SIW power dividers were simulated at two frequency ranges around 12 GHz and 24 GHz to evaluate their performance. For the 12 GHz range, simulations were conducted from 9.5 GHz to 13 GHz, while for the 24 GHz range, simulations covered 22 GHz to 26 GHz. The simulation results for the 12 GHz range are presented in Figure 4, while those for the 24 GHz range are shown in Figure 5. The simulation results for both single-layer and dual-layer designs are summarized in Table 2.

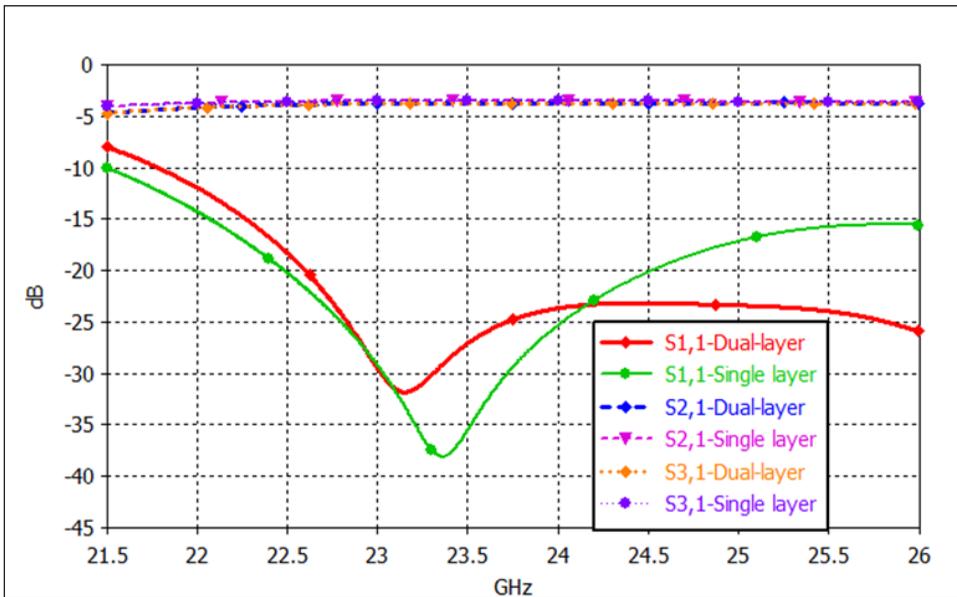


(a)

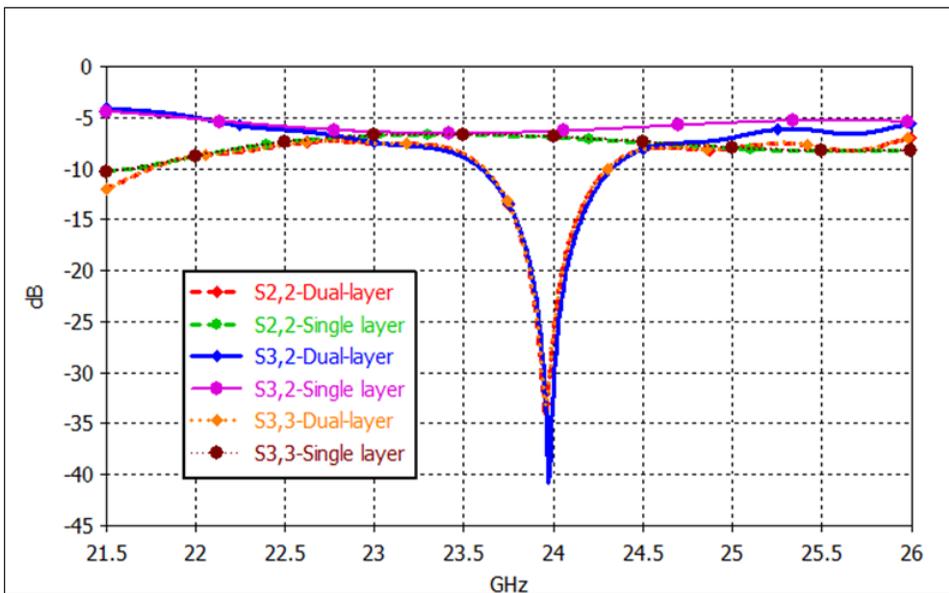


(b)

Figure 4. Simulation of S-parameters for single-layer and dual-layer SIW power dividers at 12 GHz: (a) S11, S21, and S31, (b) S22, S33, and S32



(a)



(b)

Figure 5. Simulation of S-parameters for single-layer and dual-layer SIW power dividers at 24 GHz: (a) S11, S21, and S31, (b) S22, S33, and S32

The results indicate that single-layer SIW power dividers offer a wider bandwidth but lower isolation compared to dual-layer designs. The dual-layer SIW power dividers demonstrate superior isolation performance for both the 12 GHz and 24 GHz ranges,

with maximum isolation levels of 40 dB, confirming the effectiveness of the dual-layer configuration in enhancing isolation. Additionally, the fractional bandwidth isolation at 24 GHz is better compared to 12 GHz, further highlighting the enhanced isolation capabilities at higher frequencies.

The return loss for both output ports also improves with the dual-layer design, showing a performance trend similar to isolation. This similarity arises because the introduction of a slot enhances impedance matching, reducing reflections at the output ports. The insertion loss is almost similar between the dual-layer and single-layer configurations, confirming the effectiveness of the top-layer substrate with a rectangular patch in minimizing radiation loss caused by the slot on the bottom layer.

Table 2
Simulation results of single-layer and dual-layer SIW power dividers

SIW Power Divider	10 dB isolation fractional bandwidth (GHz)	Maximum Isolation (dB)	Insertion Loss (dB)
Single-Layer at 12 GHz	NA	7	3.6 ± 0.5
Single Layer at 24 GHz	NA	5.7	3.5 ± 0.5
Dual-Layer at 12 GHz	2.90%	40	3.8 ± 0.5
Dual-Layer at 24 GHz	3.75%	40	3.7 ± 0.5

Only the 12 GHz design of the proposed SIW power divider was fabricated and tested. Figure 6 shows the fabricated device, demonstrating its layered structure.

In this design, the top layer is glued to the bottom layer, securing the two substrate layers together and ensuring structural integrity for optimal performance. Performance measurements were conducted using an Agilent E8362B vector network analyzer to

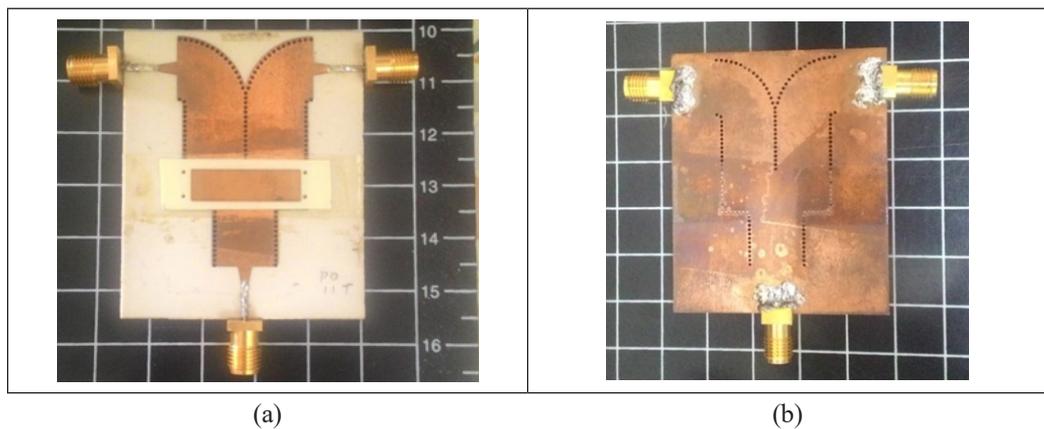


Figure 6. Photo of fabricated SIW power divider (a) top view (b) bottom view

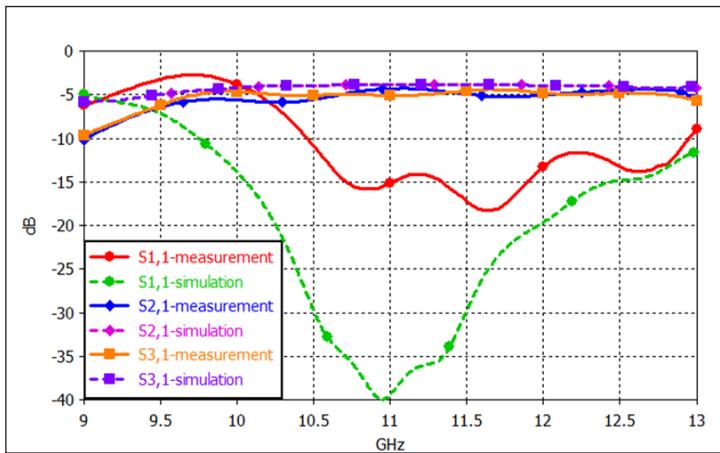
evaluate the high-frequency characteristics, and the measured results were compared to simulation data in Figure 7 to validate the design.

Measured transmission values for S_{21} and S_{31} were around 4.3 ± 0.9 dB across 10.5 GHz to 13 GHz, closely matching the simulation results and confirming effective power division between output ports. Return loss measurements indicated better than 10 dB from 9.8 GHz to 13 GHz, showing minimal reflection at the input port and confirming efficient power transmission through the device. Isolation measurements revealed that isolation between output ports exceeded 10 dB within the range of 11.8 GHz to 12.3 GHz, ensuring minimal interference between ports and supporting the device's effectiveness in signal separation.

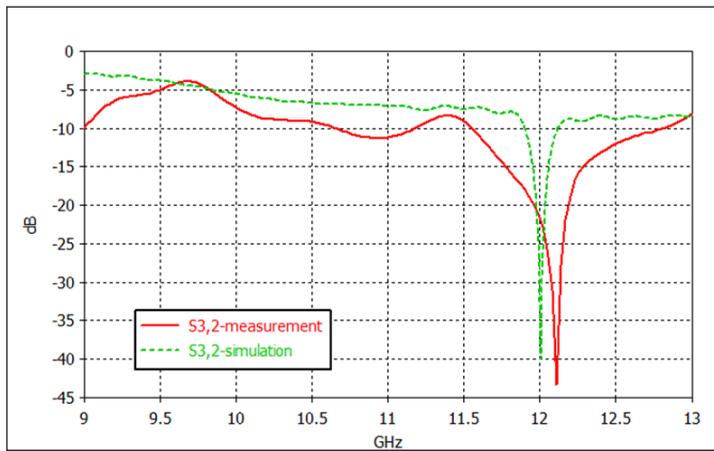
However, during the testing, it was noted that the operational frequency of both output ports was shifted towards lower frequencies compared to the simulation results. This shift can likely be attributed to fabrication errors, such as misalignment between the two substrate layers during assembly. Additionally, variations in the dimensions of the fabricated device may have introduced discrepancies between the simulation and the actual measured performance. Misalignment between the layers could alter the electromagnetic field distribution, leading to changes in the resonant behavior of the structure and, consequently, shifting the operational frequency.

In this work, a parametric study is conducted to investigate the sensitivity of key design parameters and their influence on the isolation performance of the structure. This analysis aims to identify critical dimensions that affect the isolation characteristics, providing insight into potential tuning and optimization strategies. The parametric study helps refine the design and explains the discrepancies observed between the measured and simulated results. Variations in fabrication, such as layer misalignment or dimensional inaccuracies, can lead to shifts in the isolation frequency and performance. By systematically exploring these factors, the study highlights how small deviations in key parameters can account for the observed differences, contributing to a deeper understanding of the design's behavior and enhancing the accuracy of future prototypes.

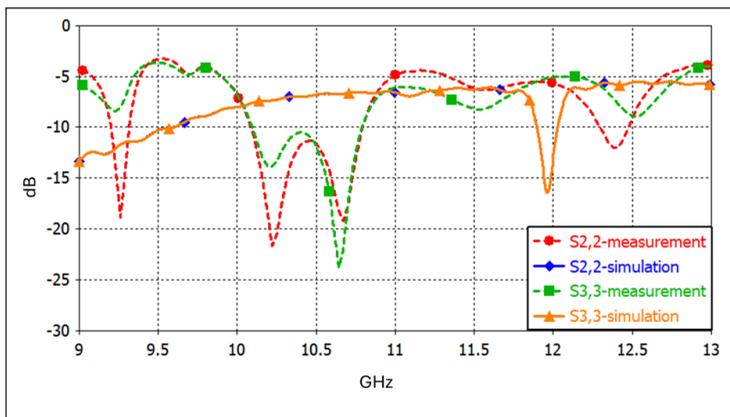
The investigation is performed to study the effects of the slot sizes and locations (S_p , S_l , and S_w) by observing their isolation performance at the 12 GHz band. For this purpose, the parameters of the copper layer on the top substrate, namely C_w , C_l and C_p are fixed at 20.2 mm, 5.9 mm and 21.5 mm, respectively. Firstly, parameters S_p and S_l are fixed at 2.8 mm and 2.1 mm, respectively, when a parametric study of S_w is performed. As depicted in Figure 8(a), the increment of S_w slightly shifts the isolation towards a lower frequency, with increased isolation levels. Meanwhile, parameters S_p and S_w are set at 2.8 mm and 11.4 mm, respectively, when S_l is studied. The increment in S_l , as shown in Figure 8(b), was also found to be slightly affecting the frequency of the peak isolation band, which shifted to 12 GHz due to the increase of the energy flow out of the slot, resulting in the increase in the isolation.



(a)

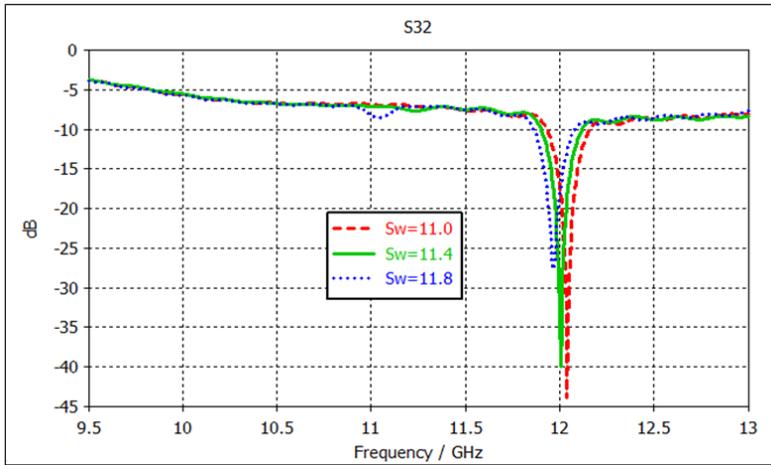


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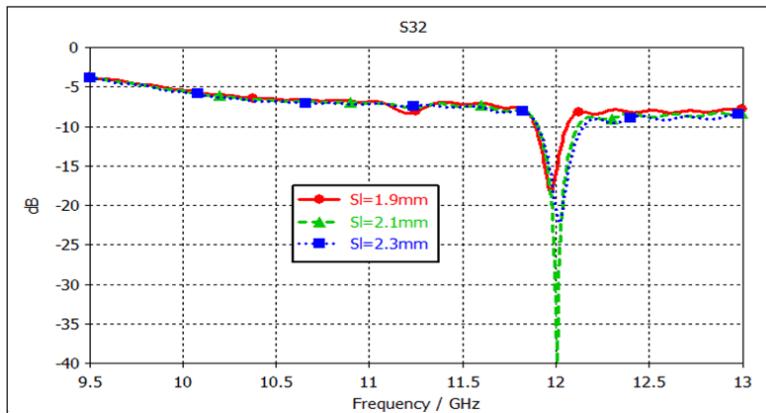


(c)

Figure 7. Comparison between simulation and measurement results (a) S_{11} , S_{21} and S_{31} (b) S_{32} , and (c) S_{22} , S_{33}



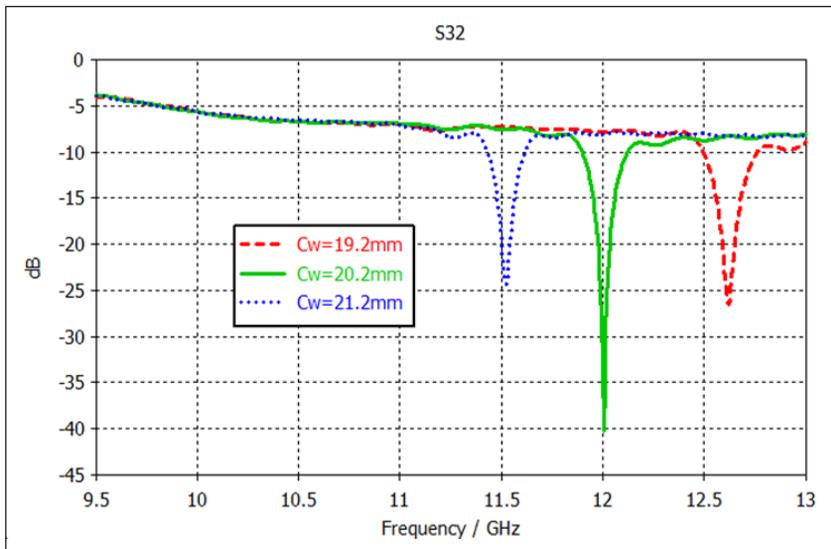
(a)



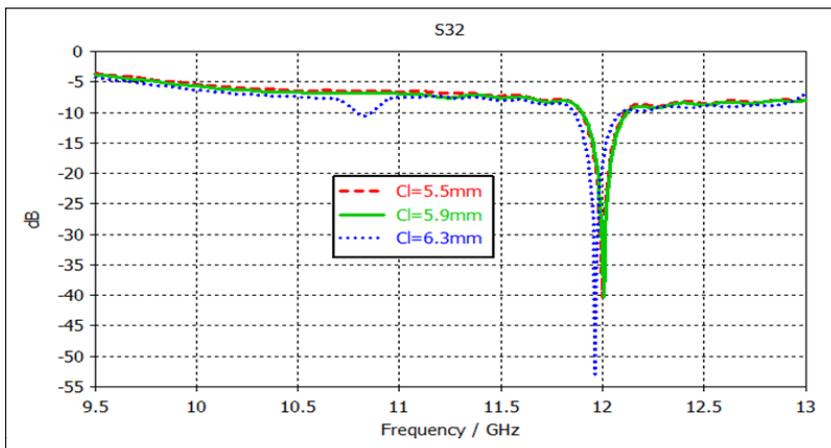
(b)

Figure 8. Simulations results of S_{22} (a) slot width, S_w and (b) slot length, S_l

Next, the dimensions of the copper layer are then studied in terms of isolation performance using parameters C_p , C_l and C_w . Parameters C_p and C_l are set at 21.7 mm and 5.9 mm, respectively, while a parametric study is performed on C_w . The increase of C_w shifts the isolation towards the lower frequency, with an isolation peak of 31 dB at $C_w = 20$ mm, due to the reduction of the resonant frequency of the top layer, as shown in Figure 9(a). Meanwhile, another parameter study is conducted to investigate the effects of C_l when parameters C_p and C_w are fixed at 21.7 mm and 20.2 mm, respectively. The simulation results shown in Figure 9(b) indicated that the increase in C_l shifted the isolation towards the lower frequencies, besides improved isolation performance due to the reduction of the resonant frequency of the top layer and increase of the energy capacity. Therefore, C_w is increased first to obtain the target frequency, followed by the optimization of C_l for the best isolation.



(a)



(b)

Figure 9. Parametric study of the proposed SIW power divider with (a) different copper widths, C_w and (b) different copper lengths, C_l

Table 3 compares this work and previous SIW Wilkinson power dividers. The proposed bi-layered power divider with a slot, as highlighted in Table 3, achieves the highest peak isolation of 43 dB, with a 10 dB isolation fractional bandwidth of 9.91%, suitable for practical applications. The insertion loss (4.2 ± 0.5 dB) and phase imbalance (5°) are comparable to other methods. At the same time, the top-layer substrate with a rectangular patch effectively minimizes radiation loss caused by the slot on the bottom layer. The design's simplicity, achieved by eliminating resistors, enhances its robustness and makes it efficient for high-frequency applications. However, it is important to acknowledge that

Table 3
Comparison between the proposed SIW power divider and other works

Reference	Technique	Peak Isolation (dB)	Peak Frequency (GHz)	10 dB isolation fractional bandwidth (%)	Insertion loss (dB)	Phase Imbalance	Resistor
(Kim et al., 2010)	Wilkinson HMSIW	19	14.5	10.82	4 ± 0.5	3.3°	1
(Djerafi et al., 2013)	Ring Wilkinson SIW	26	9.85	27.41	3.25 ± 0.5	3.3°	3
(Moulay & Djerafi, 2018)	Wilkinson with fixed width SIW line	24	10	27.13	3.3 ± 0.2	1°	8
(Yang et al., 2016)	Wilkinson HMSIW with DGS	15.3	9	39.02	4.1 ± 0.5	5.1°	1
(Yang et al., 2021)	Integrated substrate gap waveguide (ISGW)	15	26	43.38	3.53 ± 0.5	0.2°	1
(Liu et al., 2021)	Filtering power divider (FPD) on SIW	39	6.1	13.5	3.1 ± 0.2	2.3°	1
(Chi et al., 2020)	SIW filtering power divider (FPD)	20	28.2	3.54	3 ± 0.5	3.2°	2
(Yazdamanah et al., 2016)	SIW	20	4.9	4.08	4.55 ± 0.5	NA	1
(Nguyen et al., 2024)	Ku-band SIW power divider with coupled resonators	19.7	14.12	5.3	4.6	1°	None
(Huang et al., 2017)	SIW power combiner/divider with absorbing material	15	16	36	4.5 ± 0.5	±2.2°	None
(Nguyen et al., 2021)	Air-filled SIW with surface-mounted absorber	15	33.5	38.8	3.59 ± 0.51	3.71°	None
Proposed	Bi-layered with slot	43	12.1	9.91	4.2 ± 0.5	5	None

recent works, such as Nguyen et al. (2021, 2024), have demonstrated resistor-free designs with high isolation and wider fractional bandwidths. These advancements highlight ongoing efforts to optimize SIW power dividers by enhancing isolation while maintaining broad bandwidth.

CONCLUSION

In conclusion, a SIW power divider with enhanced isolation has been successfully designed at 12 GHz and 24 GHz, demonstrating the versatility of the proposed technique. Conventional SIW power dividers often face challenges in achieving high isolation and low loss without relying on lumped components, which can increase complexity and introduce additional losses. The proposed design incorporates a slot and an additional substrate layer, eliminating the need for lumped components while improving performance. The 12 GHz design was fabricated and measured, achieving good agreement with simulations. The results showed transmission values of approximately 4.2 dB, return loss better than 10 dB, and isolation exceeding 10 dB in the targeted frequency range. These results confirm the effectiveness of the proposed design for microwave systems requiring high isolation and low loss, highlighting its potential for applications in modern communication and radar technologies.

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